ABSTRACT OF THE DISCLOSURE

There is provided a semiconductor integrated circuit device wherein functional circuit groups are arranged on a chip in a direction spreads, which aims to enhance layout efficiency and to prevent deterioration of element characteristics. A unit wiring region IL1P is constituted outside of a power voltage wiring VCC, a part of a second region BIP and a unit wiring region IL1N is constituted outside of a reference voltage wiring VSS, a part of a second region BIN. Within the second wiring regions BIP and BIN, connection wirings 11, 12A, 13, 14 are wired. These connection wirings connect between units within the logic circuits CIA11, CIR12 or between the logic circuits CIR11, CIR12. There is only arranged an input/output wiring region IOL1 on a first region A1 located between the power voltage wiring VCC1 and the reference voltage wiring VSS1. Since no unit wiring region exists in the first region A1, width of the first region A1 can be laid-out short. Accordingly, connection wiring between PMOS/NMOS transistors can be shortened, areas of an N-type well region NW1 and a P-type well region PW1 can be made small. Layout efficiency and circuit characteristic can be enhanced, as a result.